



MS-7599

CPU

Ver:3.1

AMD M3 Phenom/Athlon 64 FX AM3

System Chipset

AMD RX780/RX880

ATI SB810/850

On Board Chip

FINTEK Super I/O -- F71889ED

LAN -- RTL8111DL

HD Codec --ALC892

BIOS -- SPI ROM 8M

Main Memory

DDR III X 4 (Max 8GB)

Expansion Slots

PCI-E X 16*1

PCI-E X 4 *1

PCI-E X 1 *1

PCI 2.2 Slot X 3

PWM

Controller--Intersil ISL6323 4+1 Phase

Vcore 4 Phase (MOS HIGHX2 LOWX2)

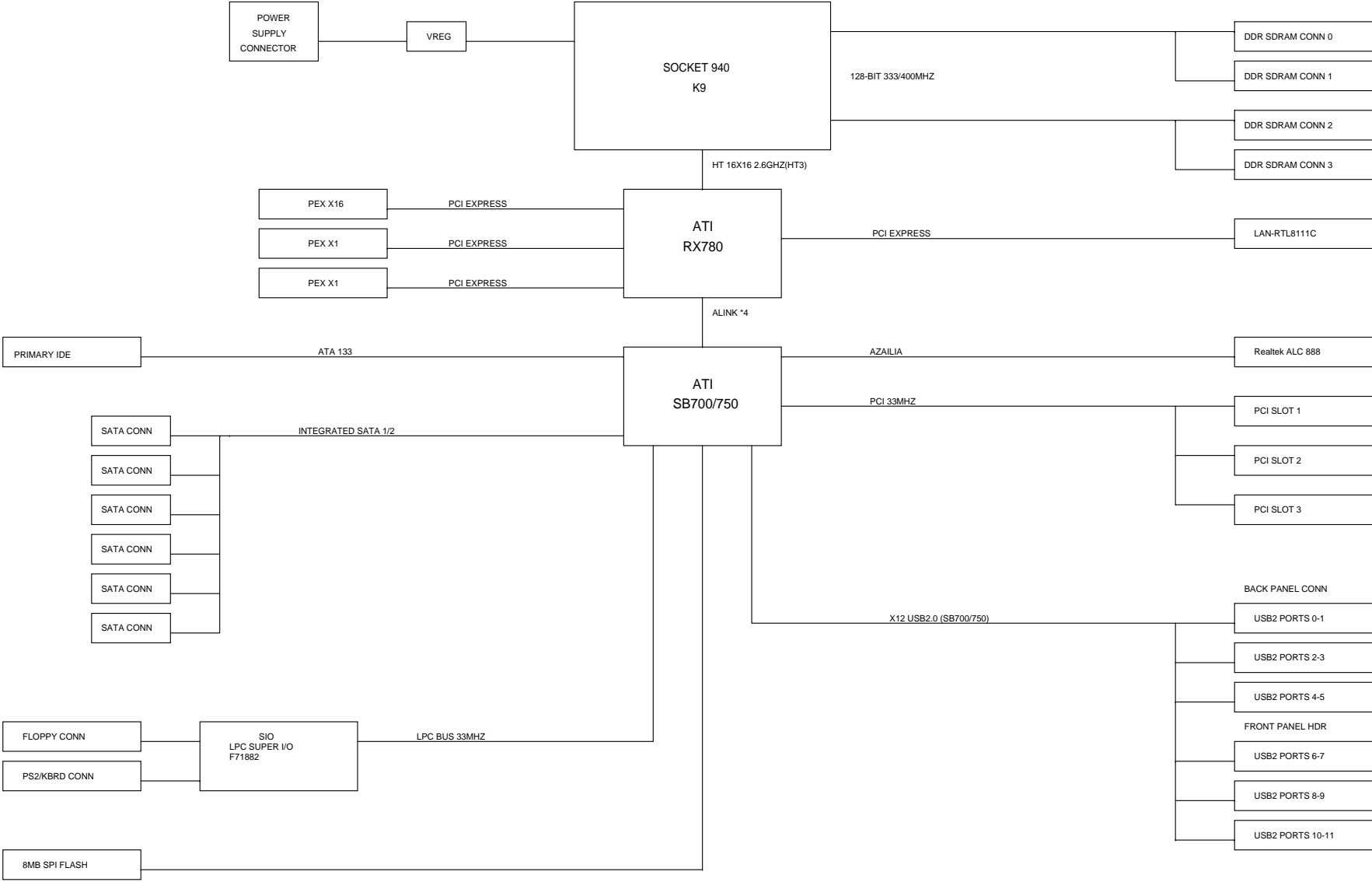
Vnb 1 Phase (MOS HIGHX1 LOWX2)

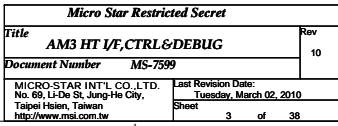
Clock Generator

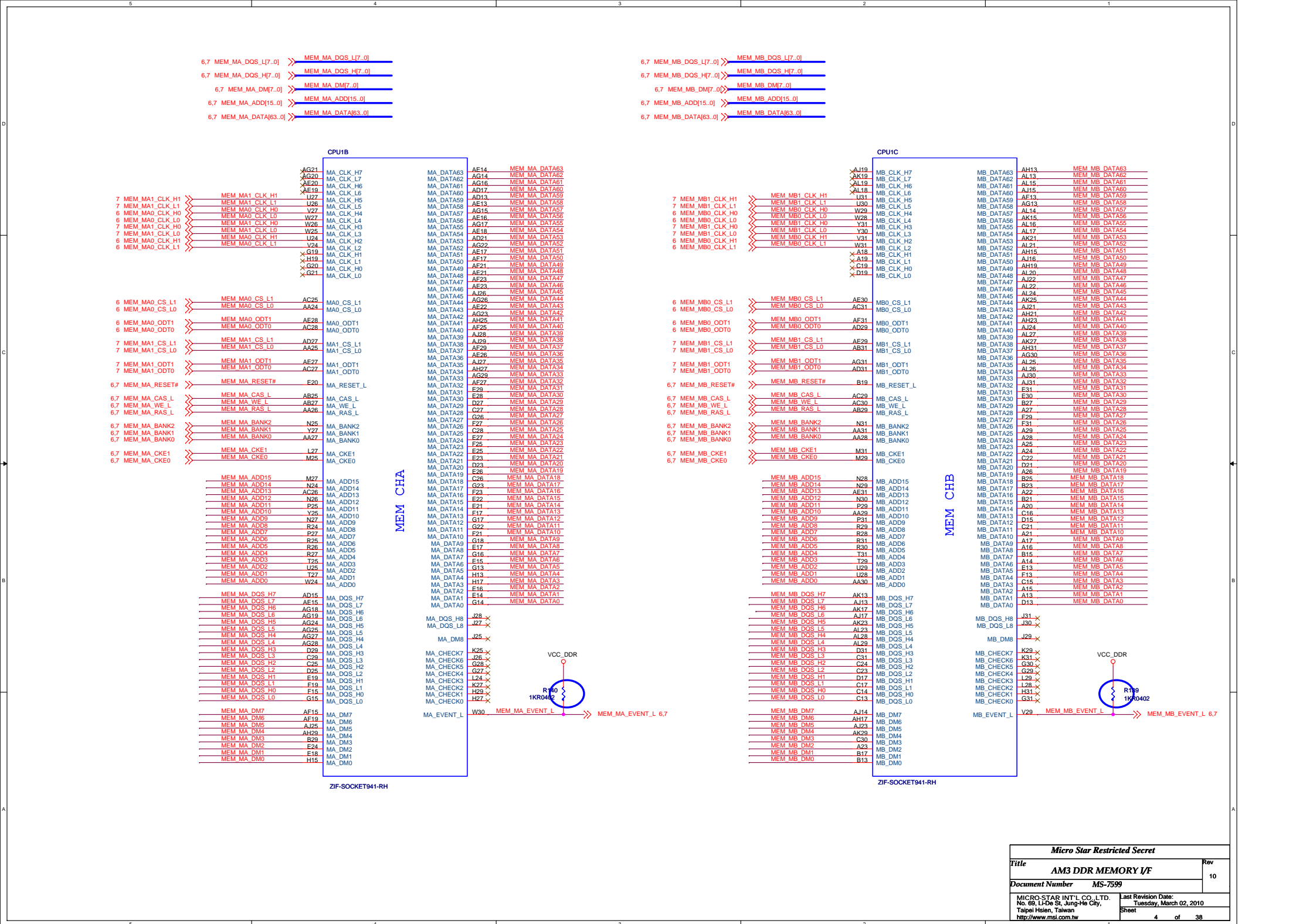
Controller--RTM880N-793

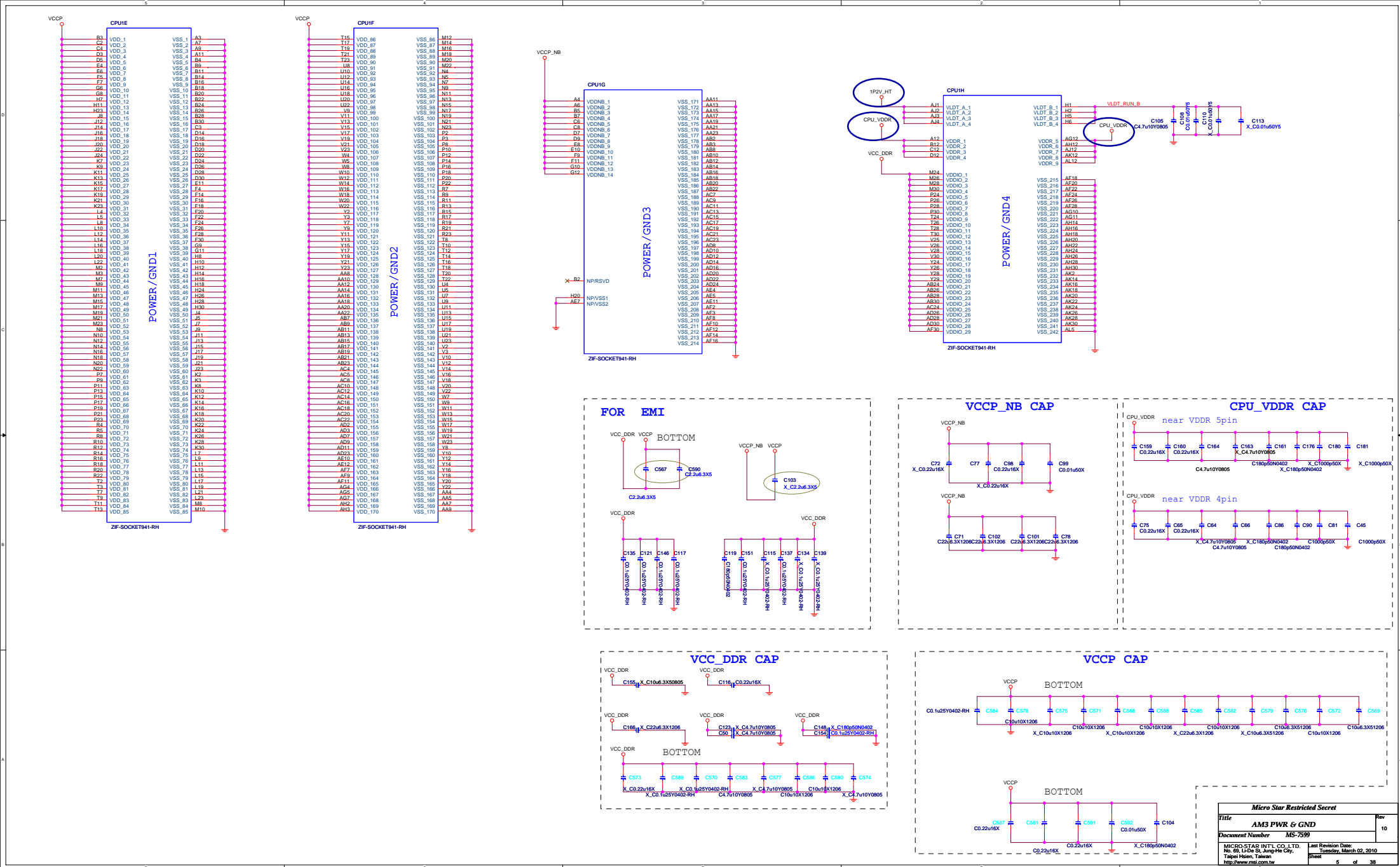
Title	Page
Cover Sheet	1
Block Diagram	2
AMD AM3 941	3-5
System Memory	6-7
ATI RX780/RX880	8-12
CLOCK GENERATOR RTM880N-793	13
ATI SB810/850	14-18
PCI Slot 1,2,3	19
PCI-E X16 Slot 2	20-21
PCI-EX4 Slot and PCI-EX1 Slot	21
LAN RTL8111DL	22
HD Audio - ALC892	23
IDE&FAN	24
UPI ACPI	25
USB connectors	26
I/O F71889ED / FDD	27
ATX Connector&Front Panel& KB	28
PWM - ISL6323A	29
VCC_DDR&1P1V_CORE	30
MANUAL PARTS	31
JMB368 IDE	32
NEC720200 USB3.0	33
POWER MAP	34
POWER OK MAP	35
Clock Map	36
RESET MAP&Power Sequence	37
	38

BLOCK DIAGRAM









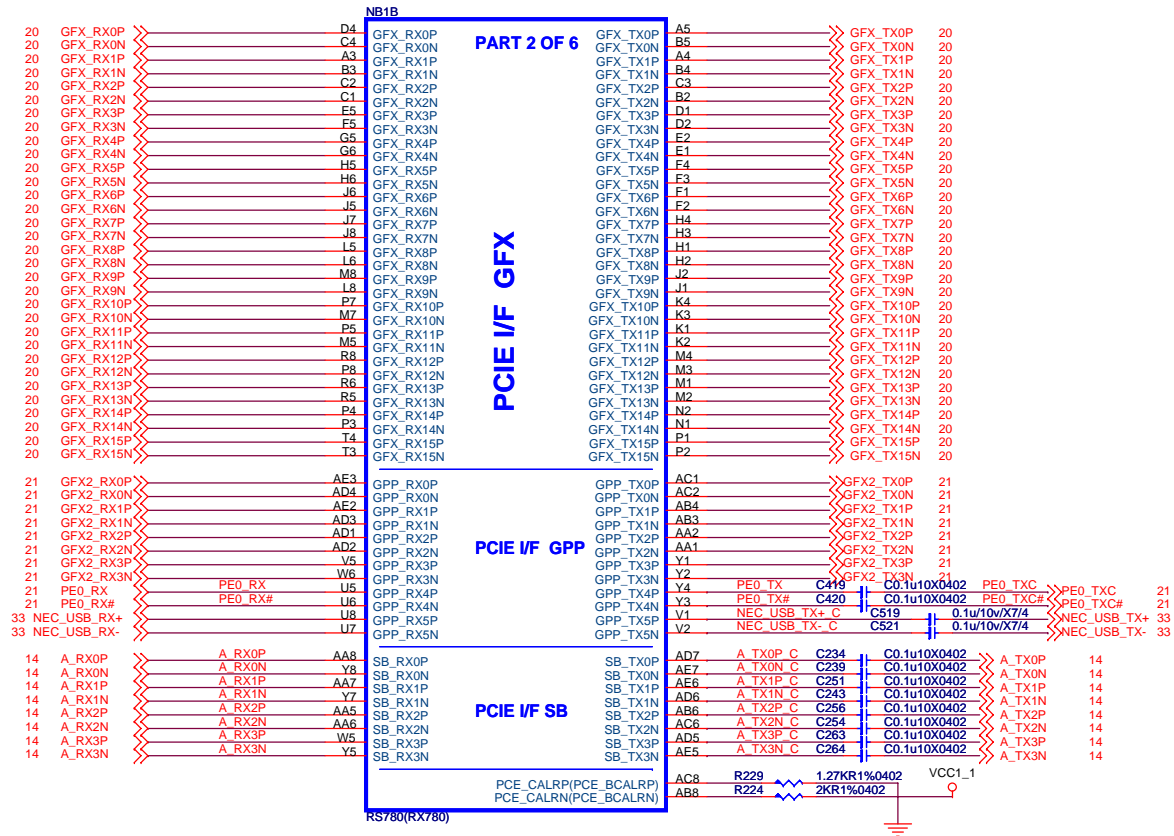
3 HT_CADIN_H[15..0] >> HT_CADIN_H[15..0]
3 HT_CADIN_L[15..0] >> HT_CADIN_L[15..0]
3 HT_CADOUT_H[15..0] >> HT_CADOUT_H[15..0]
3 HT_CADOUT_L[15..0] >> HT_CADOUT_L[15..0]



RX780/RS740/RS780 difference table (HT LINK)

SIGNALS	RS740	RX780	RS780
HT_RXCALP	49.9R (GND)	1.21K	301R
HT_RXCALN	49.9R (VDDHT)		
HT_TXCALP	100R	1.21K	301R
HT_TXCALN			

Micro Star Restricted Secret		
Title	RD780-HT LINK I/F	Rev
Document Number	MS-7599	10
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, March 02, 2010
Sheet		8 of 38

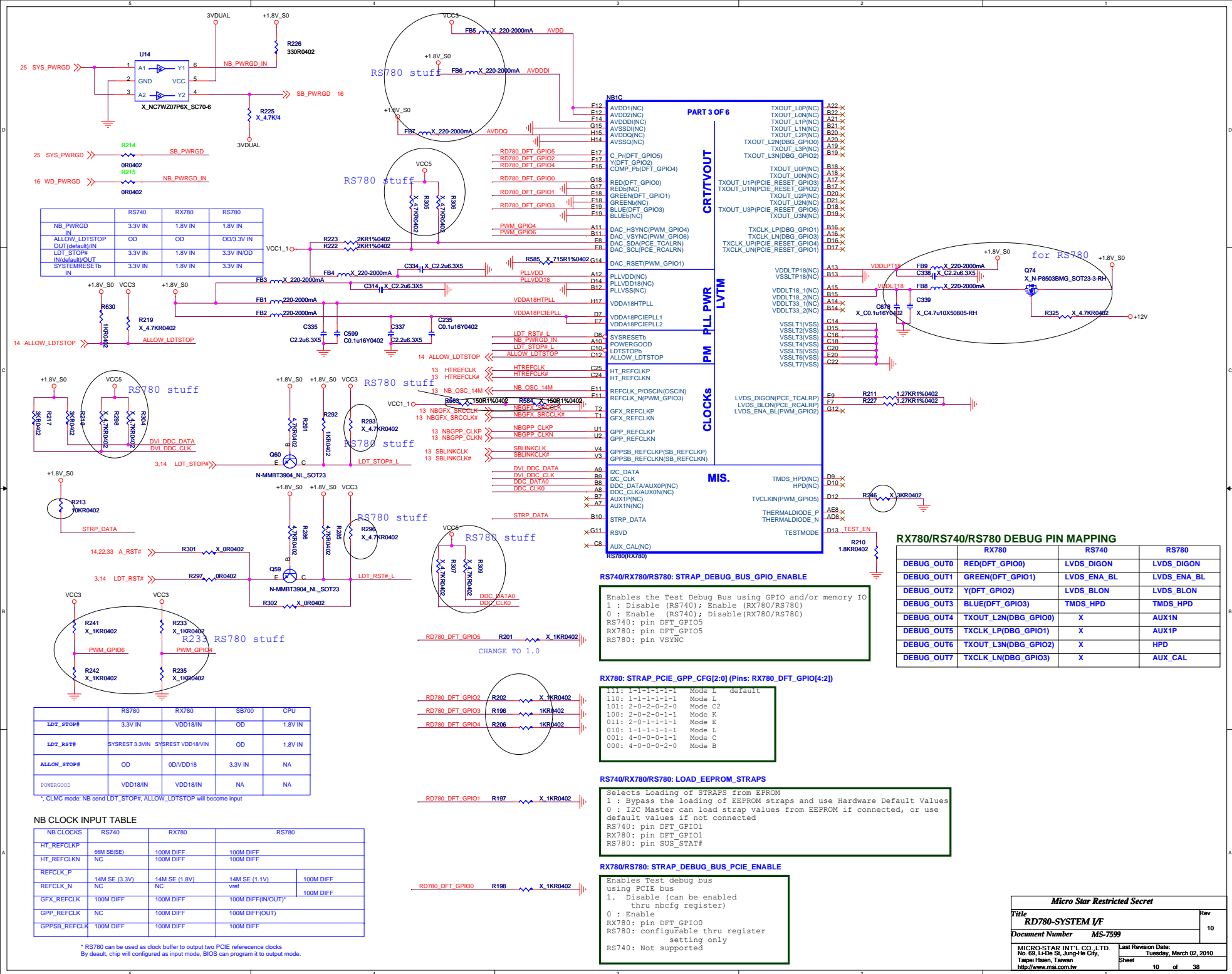


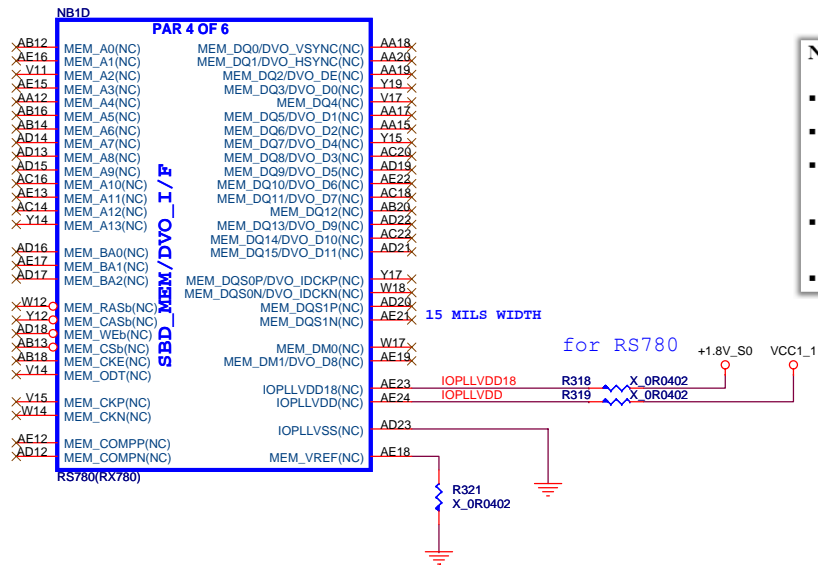
RX740/RS740/RS780 difference table (PCIE LINK)

	RS740	RX740/RS780
PCE_CALRP	562R (GND)	1.27K (GND)
GPP4	NC	GPP4
GPP5	NC	GPP5

RS780 Display Port Support (muxed on GFX)

DP0	GFX_TX0,TX1,TX2 and TX3 AUX0 and HPD0
DP1	GFX_TX4,TX5,TX6 and TX7 AUX1 and HPD1

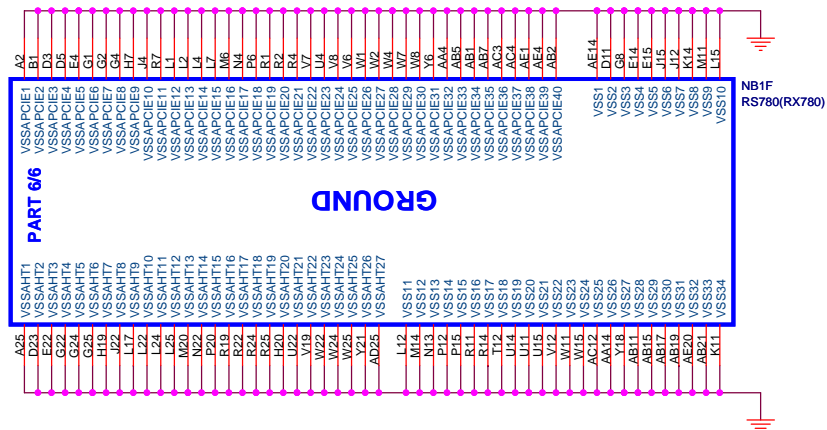




Note: If the Side-port memory interface is **not** used, make sure that:

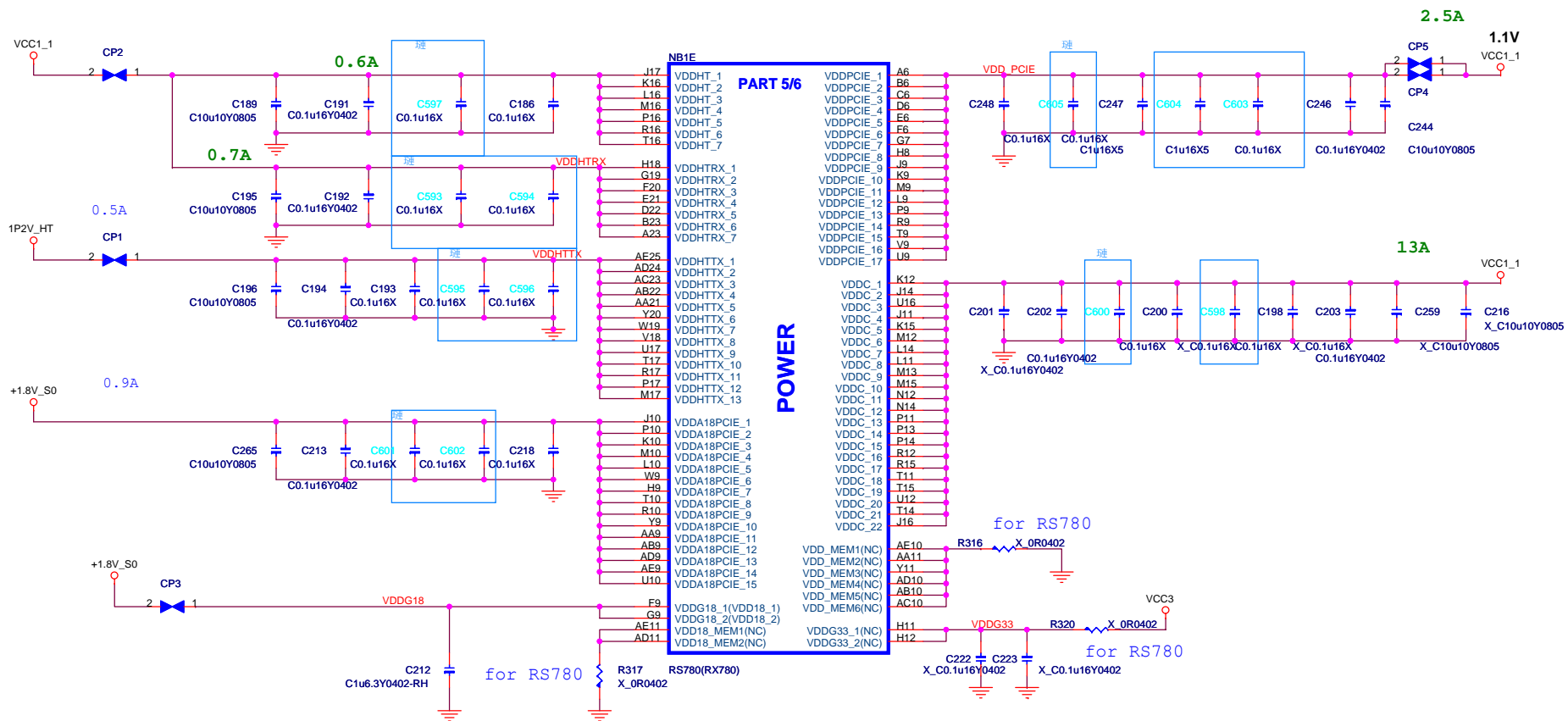
- The memory interface IO power (VDD_MEM) is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface IO transform power (VDD18_MEM) is connected to 1.8 V.
- The voltage divider for memory interface reference voltage MEM_VREF is connected to 1.5 V for DDR3 or 1.8 V for DDR2.
- The memory interface PLL power IOPLLVD18 is connected to 1.8 V and IOPLLVD is connected to 1.2 V for the RS740 and to 1.1 V for the RS780.
- The memory interface enable strap DFT_GPIO0 is **not** connected to the GND.

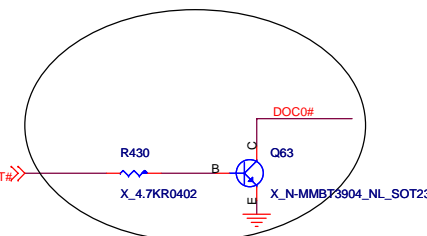
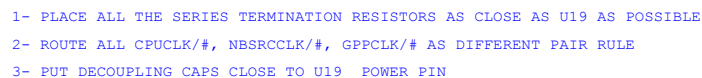
Micro Star Restricted Secret		
Title	RD780-SPMEM/STRAPS	Rev
Document Number	MS-7599	10
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St., Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, March 02, 2010
		Sheet 11 of 38



RS740/RX780/RS780 POWER DIFFERENCE TABLE

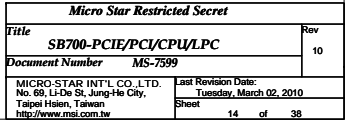
PIN NAME	RS740	RX780	RS780	PIN NAME	RS740	RX780	RS780
VDDHT	NC	+1.1V	+1.1V	IOPLLVD	+1.2V	NC	+1.1V
VDDHTRX	NC	+1.1V	+1.1V	AVDD	+3.3V	NC	+3.3V
VDDHTTX	+1.2V	+1.2V	+1.2V	AVDDDI	+1.8V	NC	+1.8V
VDDA18PCIE	NC	+1.8V	+1.8V	AVDDQ	+1.8V	NC	+1.8V
VDD18	+1.8V	+1.8V	+1.8V	PLLVD	+1.2V	NC	+1.1V
VDD18_MEM	NC	NC	+1.8V	PLLVDD18	+1.8V	NC	+1.8V
VDDPCIE	+1.2V	+1.1V	+1.1V	VDDA18PCIEPLL	+1.2V	+1.8V	+1.8V
VDDC	+1.2V	+1.1V	+1.1V	VDDA18HTPLL	+1.8V	+1.8V	+1.8V
VDD_MEM	+1.8V/1.5V	NC	+1.8V/1.5V	VDDLT18	+1.8V	NC	+1.8V
VDD33	+3.3V	NC	+3.3V	VDDLTP18	+1.8V	NC	+1.8V
IOPLLVD18	+1.8V	NC	+1.8V	VDDLTP33	+3.3V	NC	NC

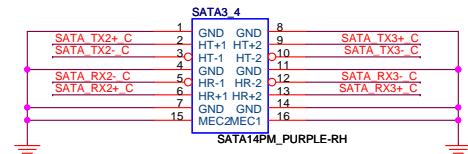
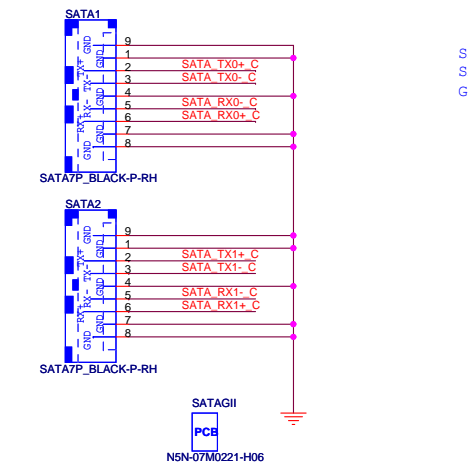




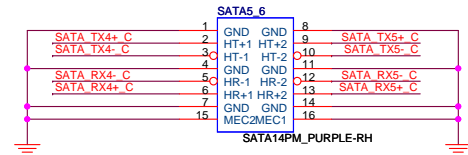
```
SEL_HTT66 : 'L' 100Mhz FOR 780
           'H' 66Mhz FOR 740
```



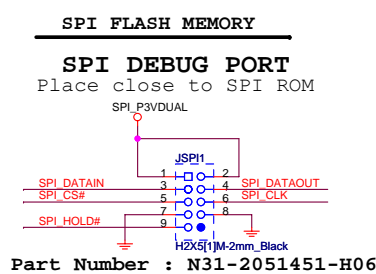
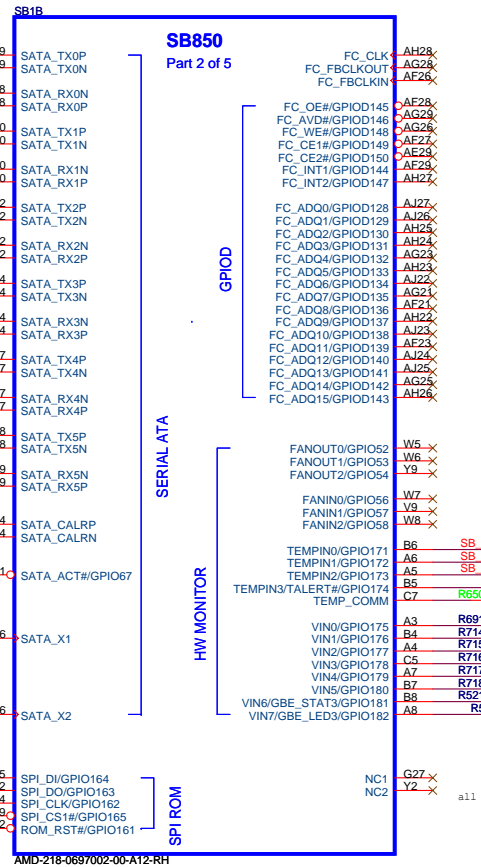
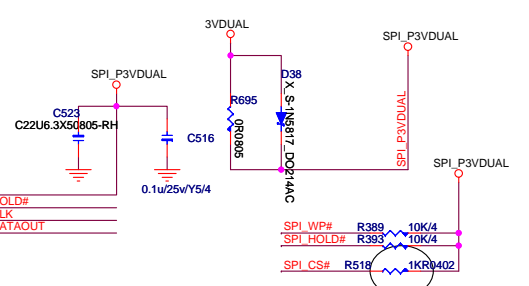
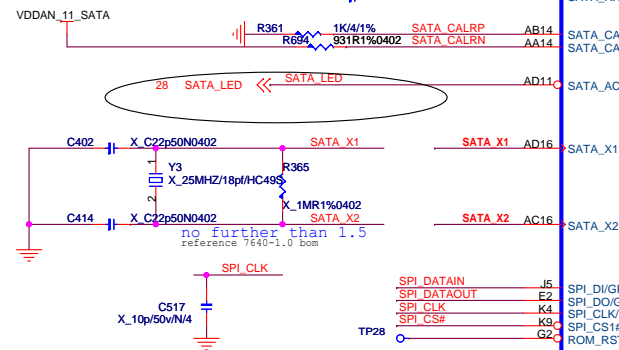
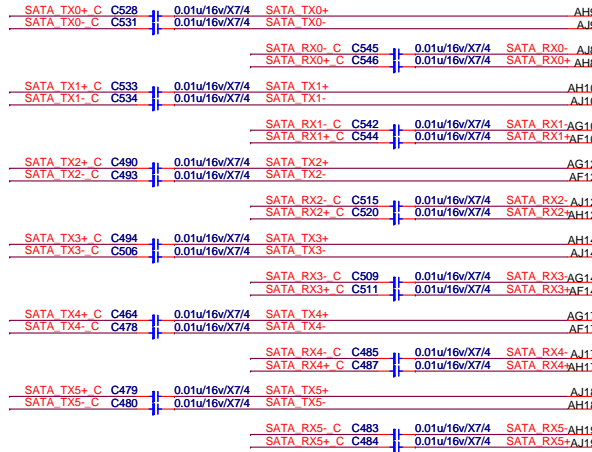


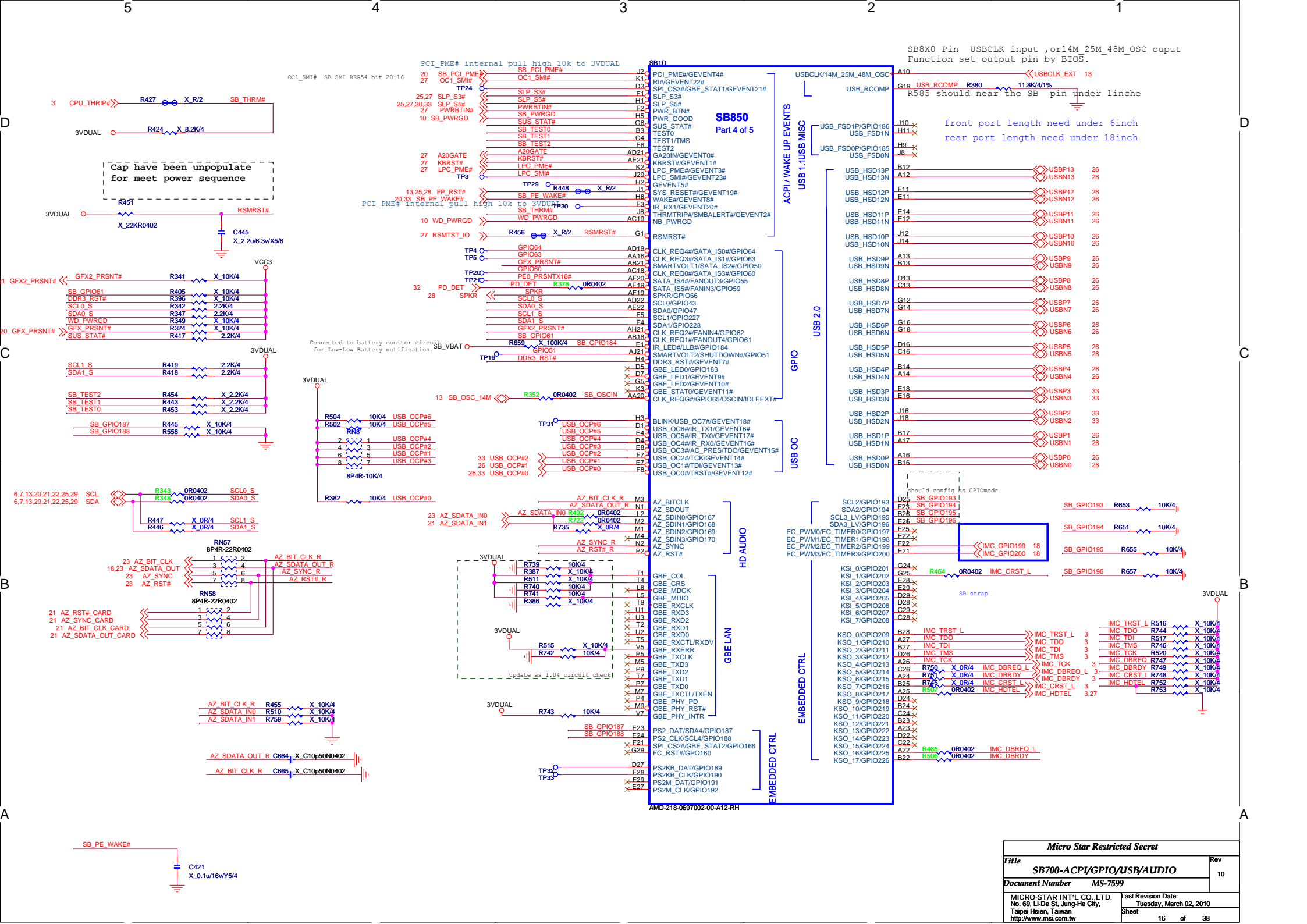


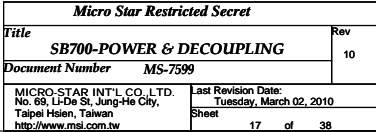
N5N-07M0231-H06



SATA_TX[5:0]P/N: Routed with 100-ohm \pm 10% differential impedance.
SATA_RX[5:0]P/N: Routed with 90-ohm \pm 10% differential impedance.
Gen3: Signal length from the Southbridge to connector \leq 3.0".

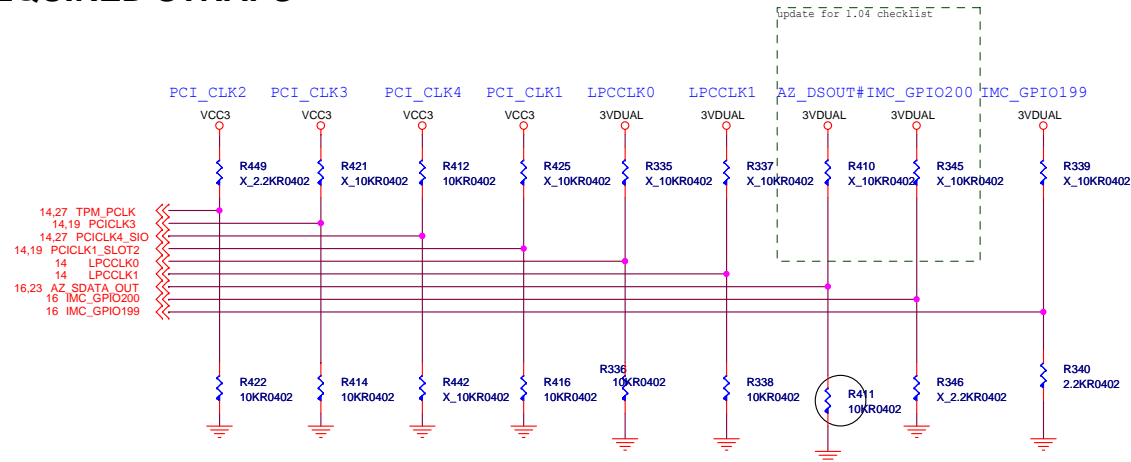






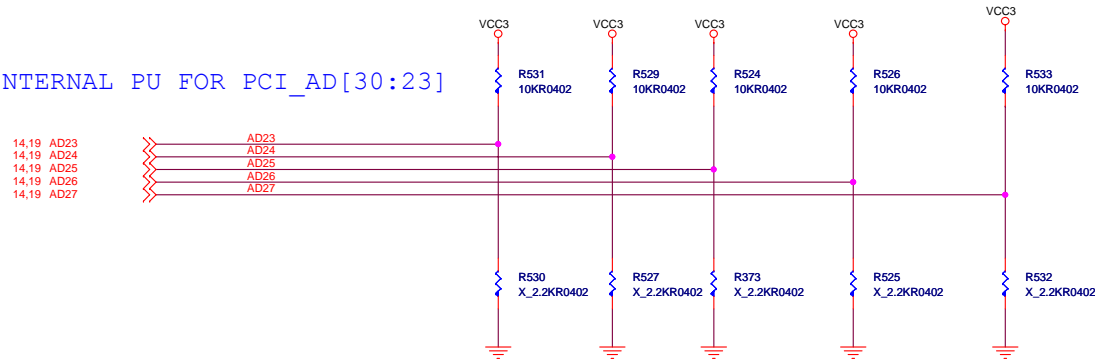
REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK



	PCI_CLK1	PCI_CLK2	PCI_CLK3	PCI_CLK4	LPC_CLK0	LPC_CLK1	AZ_DSOUT#	IMC_GPIO200	IMC_GPIO199
PULL HIGH	ALLOW PCIE GEN2	WATCHDOG TIMER ON NB_PWRGD ENABLED	USE DEBUG STRAPS	NON-FUSION CPU CLOCK MODE DEFAULT	CLKGEN ENABLE	CLKGEN ENABLED		ROM TYPE: H, H = Reserved H, L = SPI ROM DEFAULT	
PULL LOW	FORCE PCIE GEN1 DEFAULT	WATCHDOG TIMER ON NB_PWRGD DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT	FUSION CPU CLOCK MODE DEFAULT	DISABLE EC DEFAULT	CLKGEN DISABLED DEFAULT	PERFORMANCE MODE DEFAULT	L, H = LPC ROM L, L = FWH ROM	

SB800 HAS 15K INTERNAL PU FOR PCI_AD[30:23]

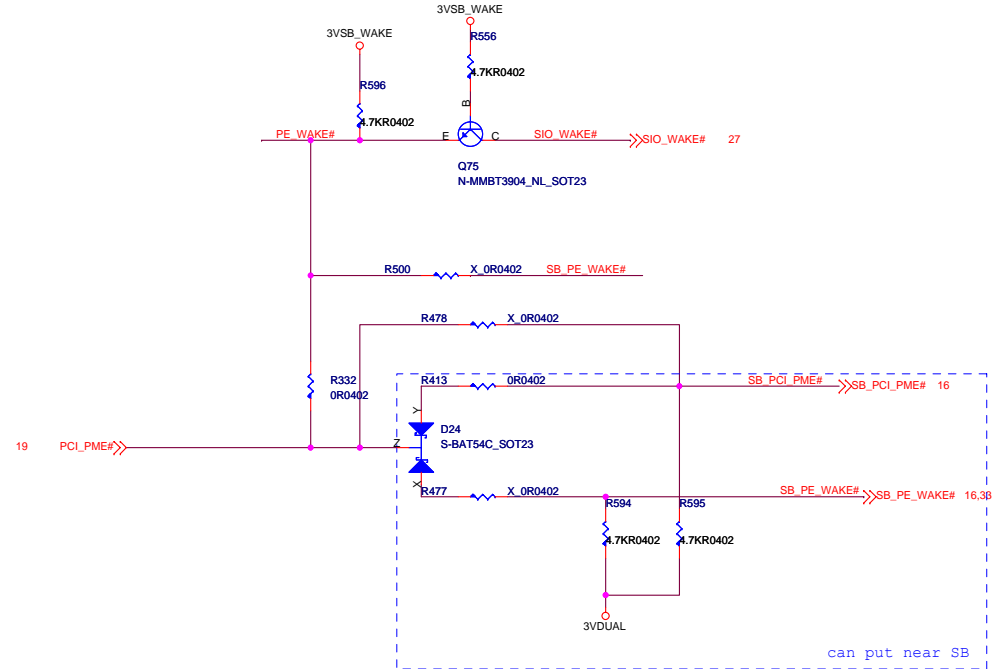
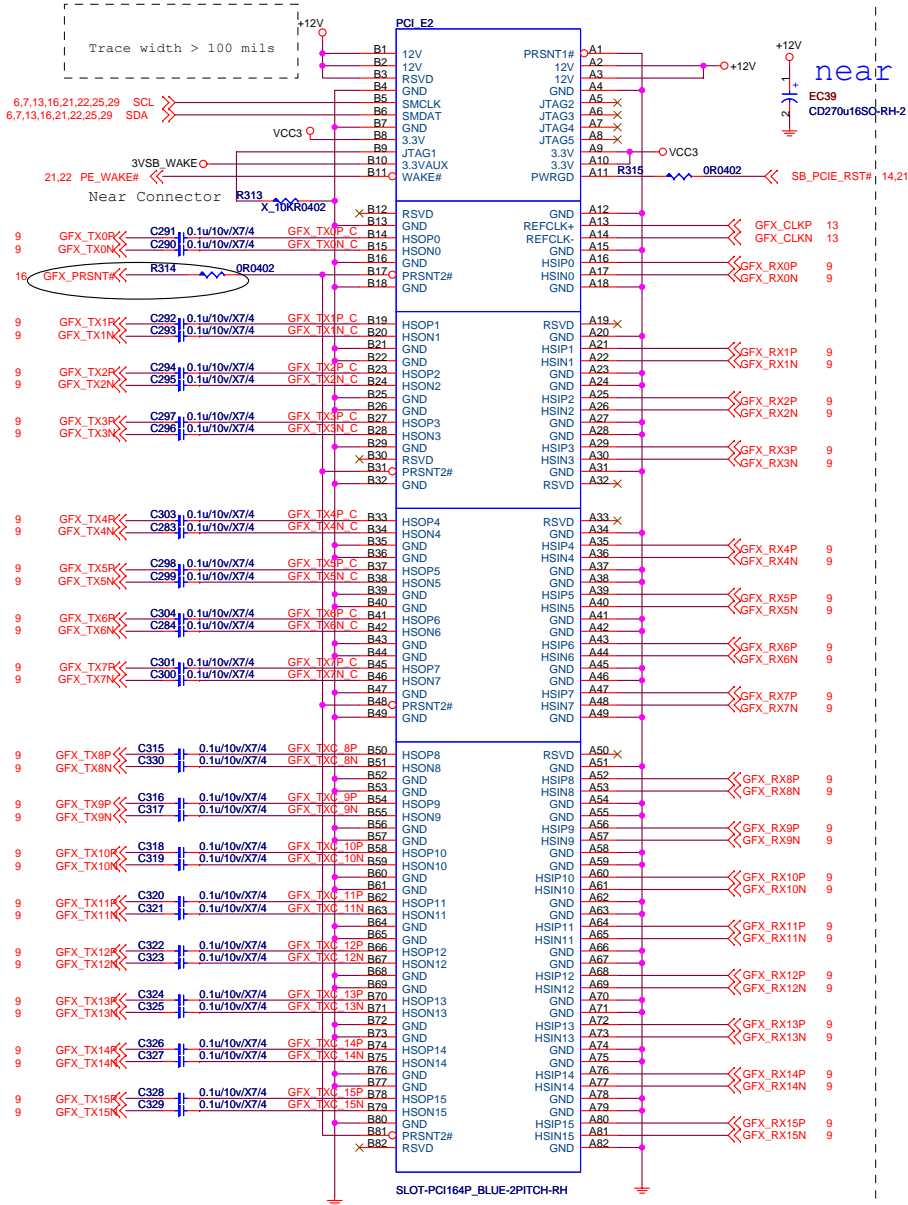


DEBUG STRAPS

	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE PCI PLL DEFAULT	DISABLE ILA AUTORUN DEFAULT	USE FC PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	DISABLE PCI MEM BOOT DEFAULT
PULL LOW	BYPASS PCI PLL	ENABLE ILA AUTORUN	BYPASS FC PLL	USE EEPROM PCIE STRAPS	ENABLE PCI MEM BOOT

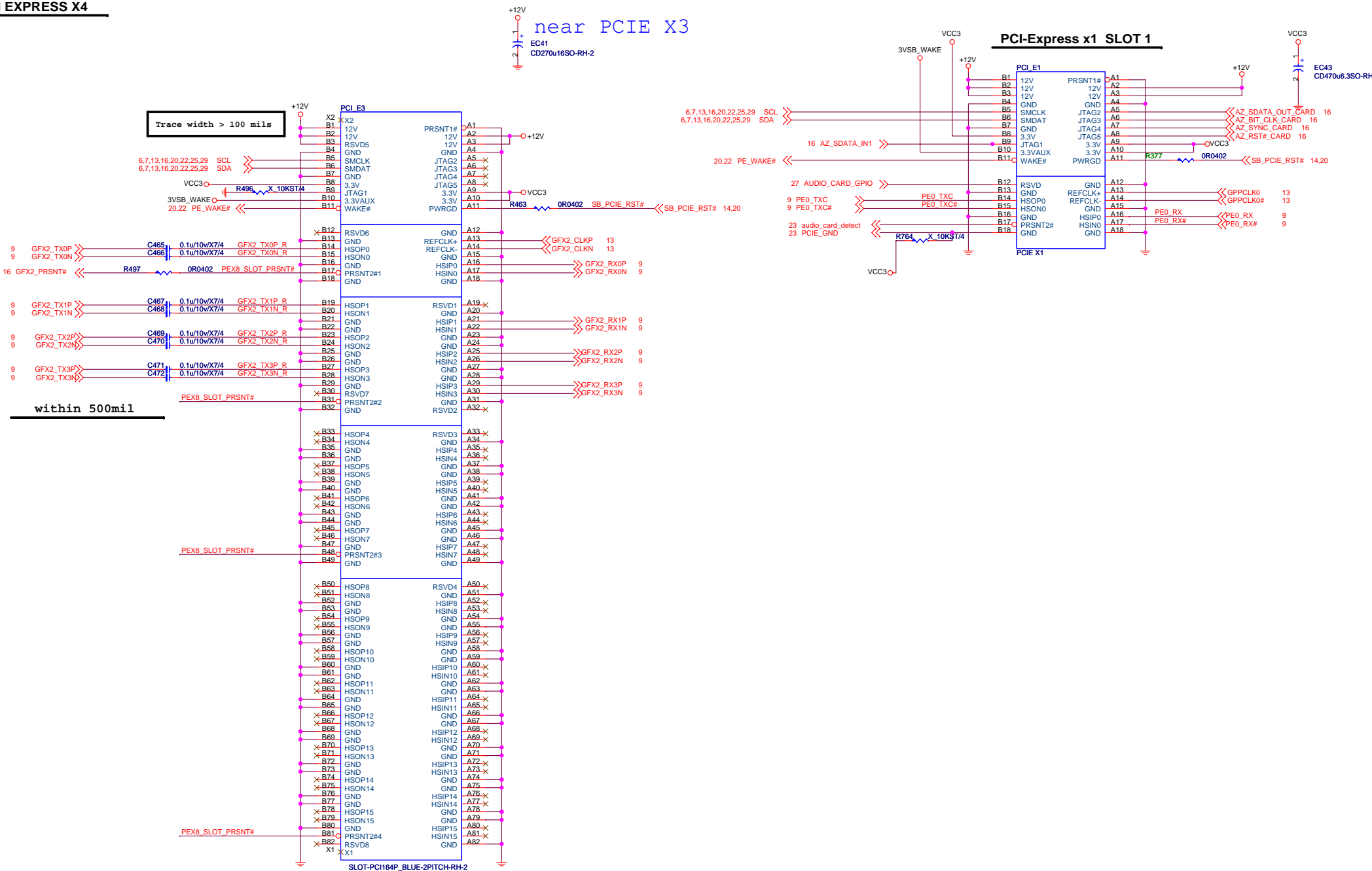
Micro Star Restricted Secret		
Title	SB700-STRAPS	Rev 10
Document Number	MS-7599	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-Ho City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, March 02, 2010 Sheet 18 of 38

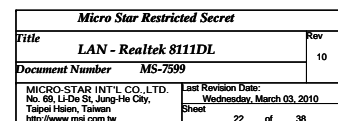
PCI EXPRESS_16

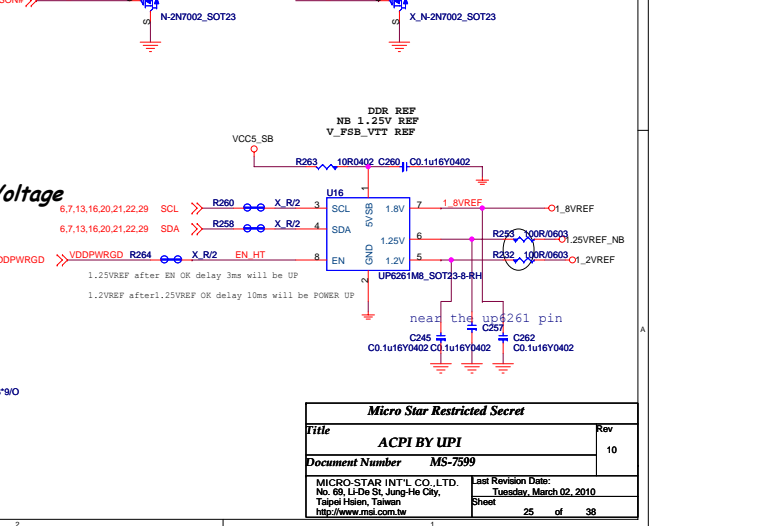
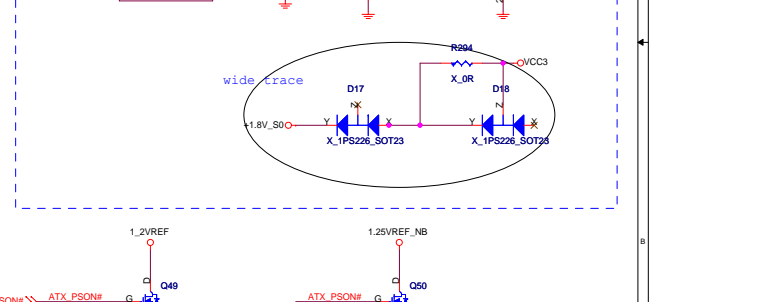
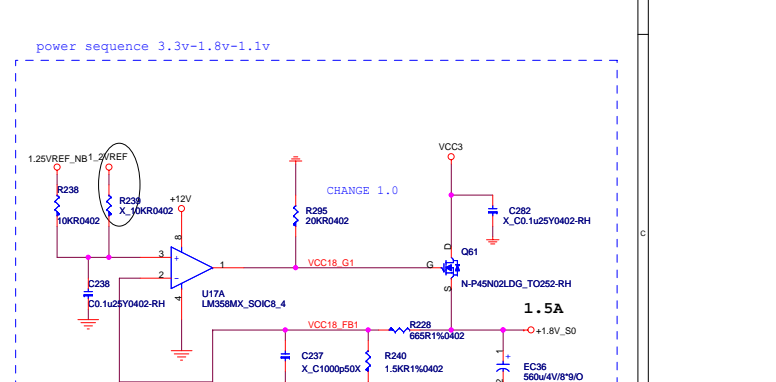
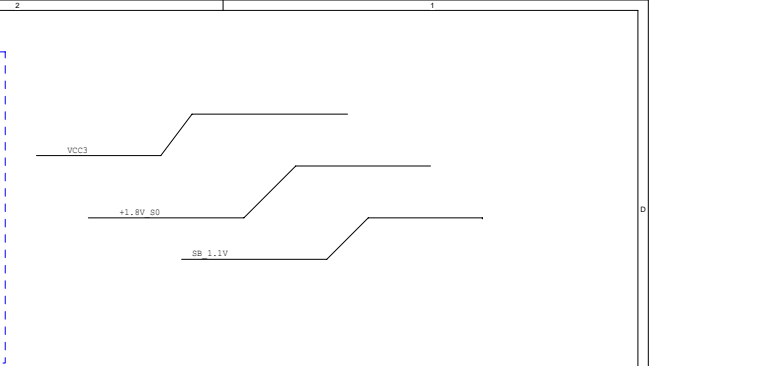
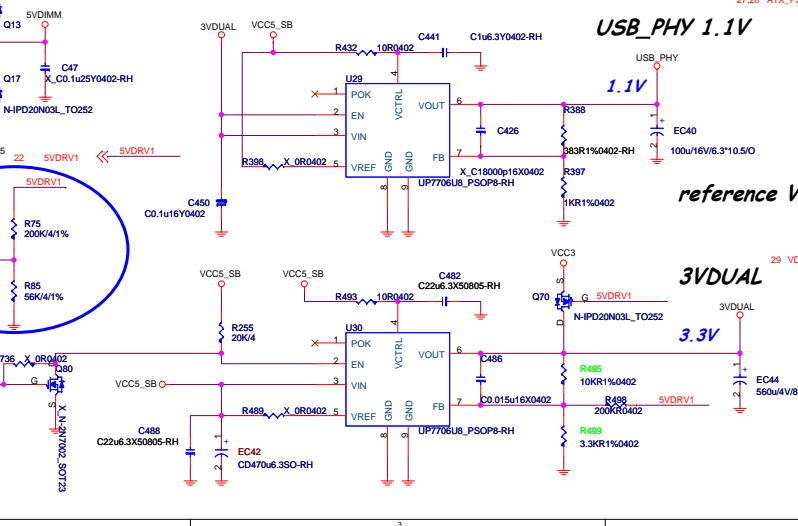
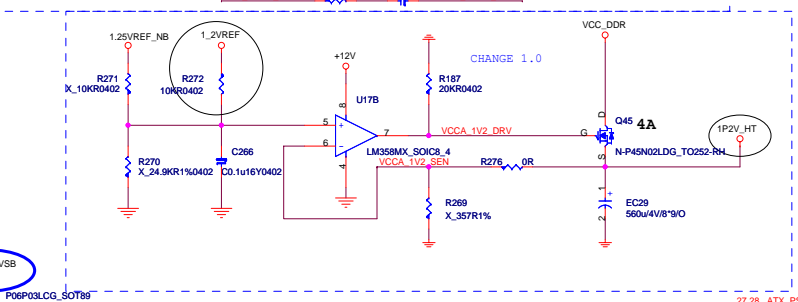
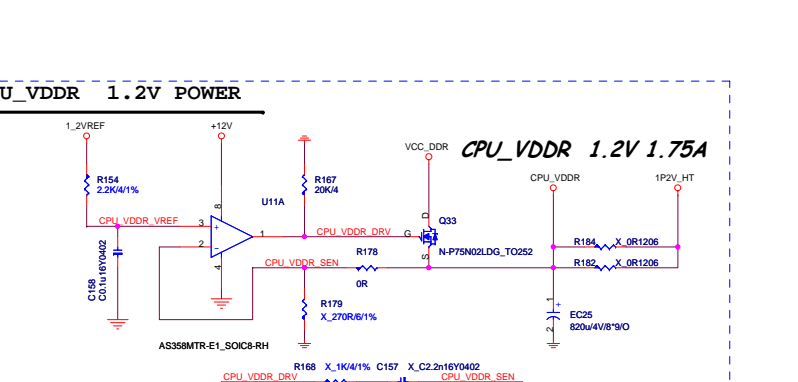
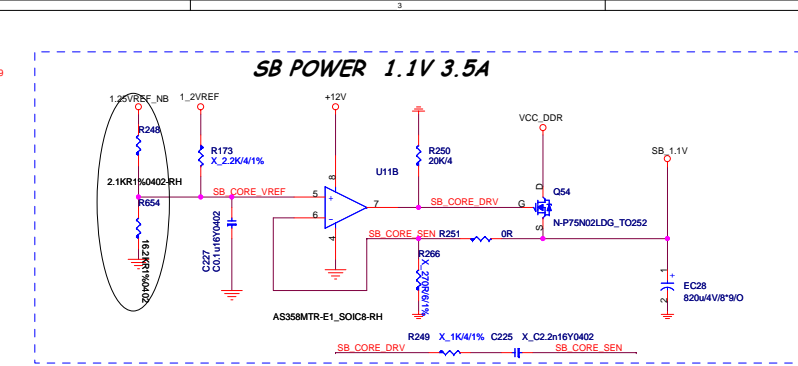
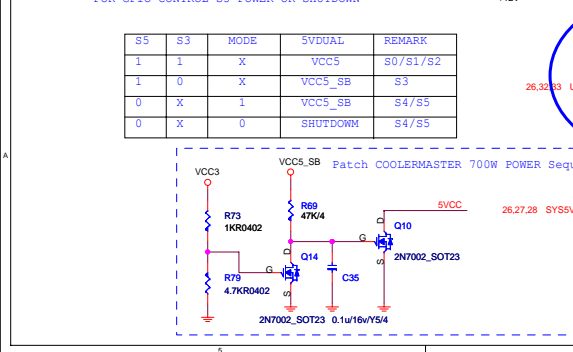
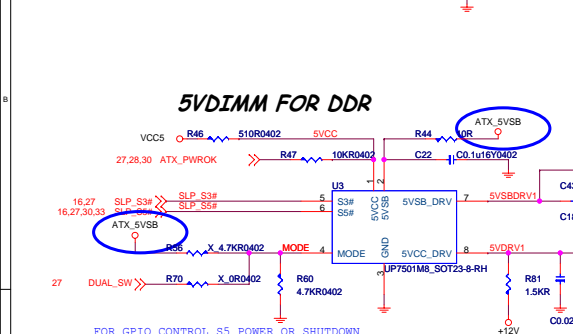
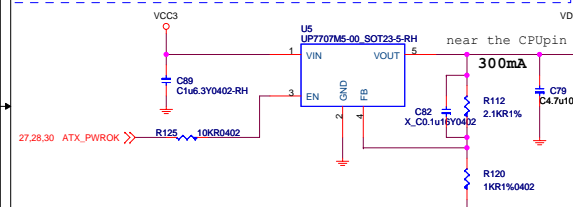
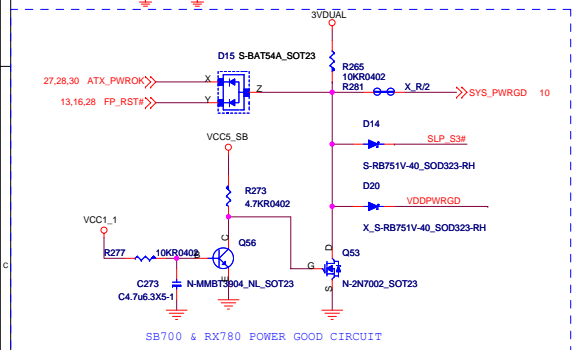
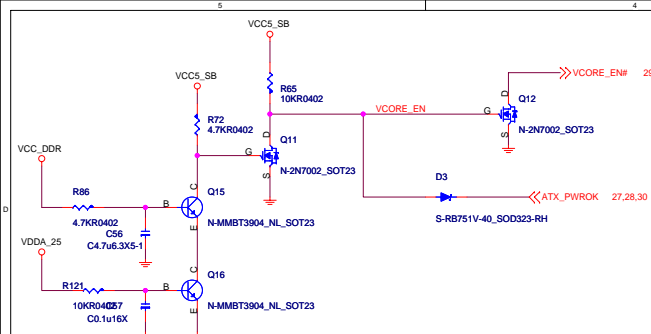


Digital Switch		SEL pin		SLI function	
SEL (X8 X8#)	Output	X8 SW	PCI-E Slot 1/2		
Low	0a	Low	X8 / X8		
Hi	0b	Hi	X16 / 0		

PCI EXPRESS X4





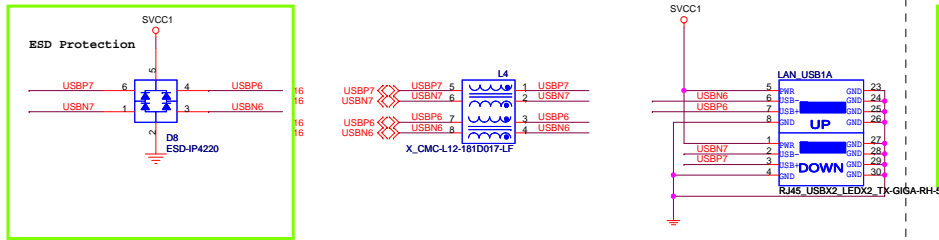


5VDDIMM FOR DDR

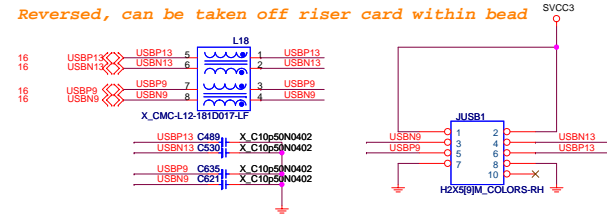
S5	S3	MODE	5VDDUAL	REMARK
1	1	X	VCC5	S0/S1/S2
1	0	X	VCC5_SB	S3
0	X	1	VCC5_SB	S4/S5
0	X	0	SHUTDOWN	S4/S5

FOR GPIO CONTROL S5 POWER OR SHUTDOWN

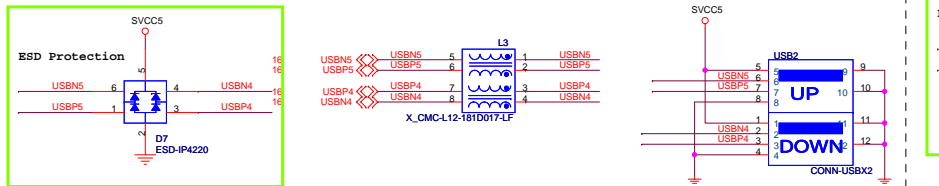
REAR PANEL USB CONNECTOR FOR USB PORT 0,1



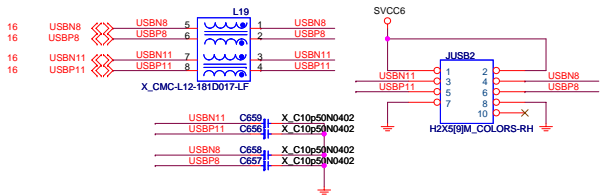
FRONT PANEL USB CONNECTOR FOR USB PORT 6,7



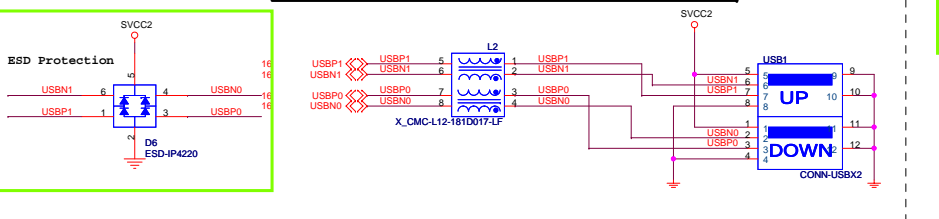
REAR PANEL USB CONNECTOR FOR USB PORT 2,3



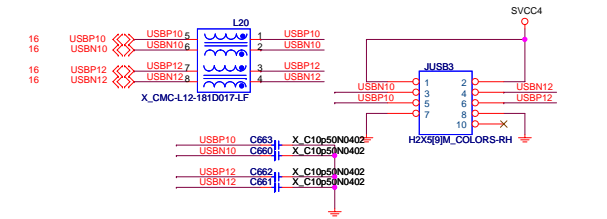
FRONT PANEL USB CONNECTOR FOR USB PORT 8,9



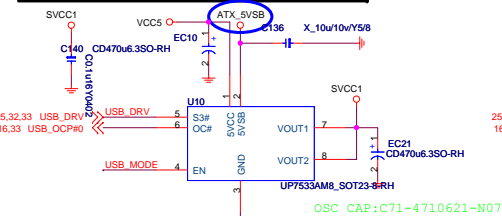
REAR PANEL USB CONNECTOR FOR USB PORT 4,5



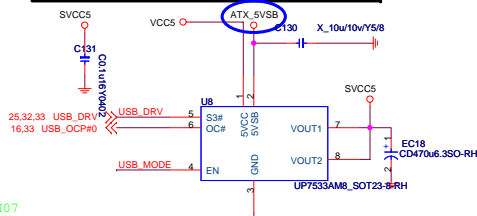
FRONT PANEL USB CONNECTOR FOR USB PORT 10,11



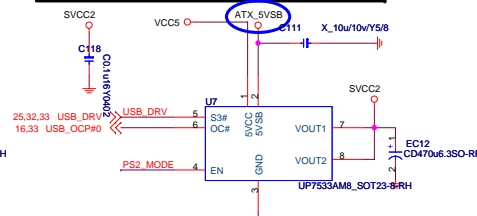
POWER CIRCUIT FOR USB PORT 0,1



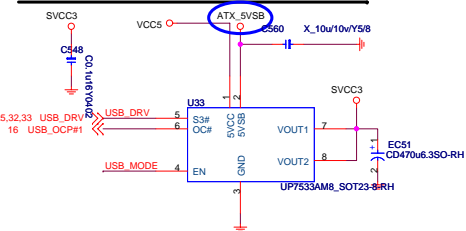
POWER CIRCUIT FOR USB PORT 2,3



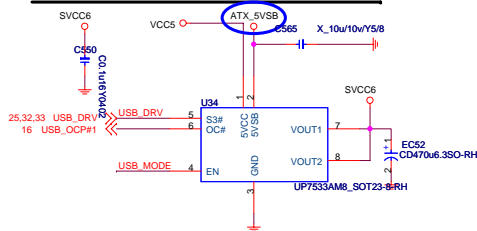
POWER CIRCUIT FOR USB PORT 4,5



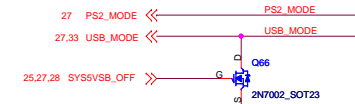
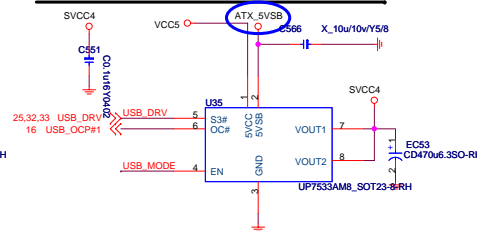
POWER CIRCUIT FOR USB PORT 6,7



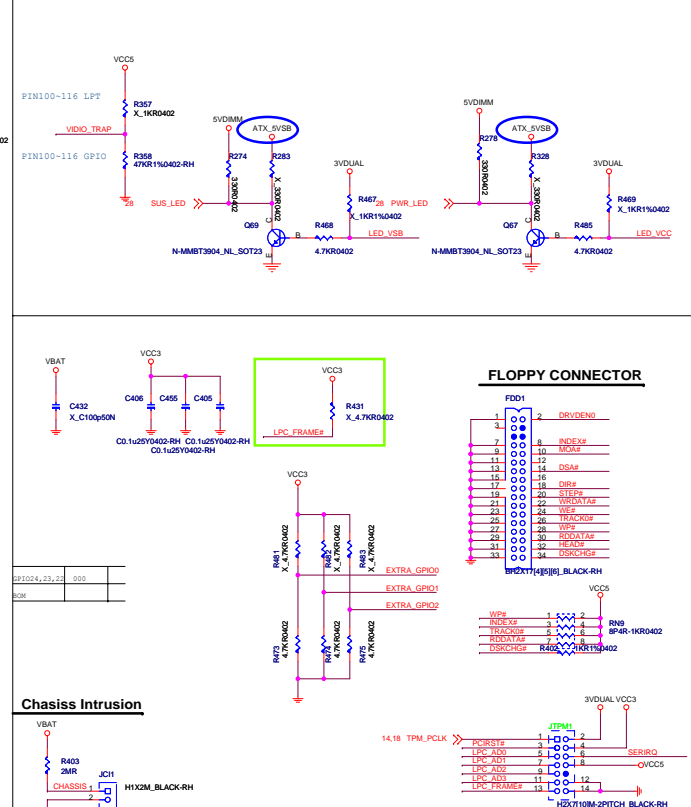
POWER CIRCUIT FOR USB PORT 8,9



POWER CIRCUIT FOR USB PORT 10,11



Micro Star Restricted Secret	
Title	Rev
USB CONNECTORS	10
Document Number	MS-7599
MICRO-STAR INT'L CO. LTD.	
No. 69, Li-De St, Jung-Hsi City,	
Taipei Hsien, Taiwan	
http://www.msi.com.tw	
Last Revision Date:	
Tuesday, March 02, 2010	
Sheet	26 of 38



	Don't STUFF	STUFF
RTS2#	PMW FAN	LINEAR FAN
RTSA#	80FPort enable	80FPort disable
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
DTR2	PIN151-56 as GPIO	PIN151-56 as BUS I/F
SOUT2	PIN151-56 as GPIO	PIN151-56 as BUS I/F

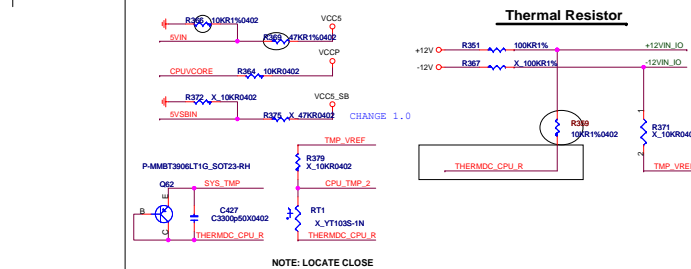
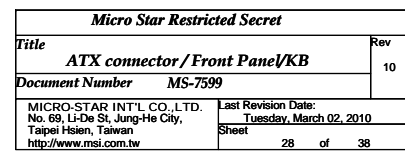
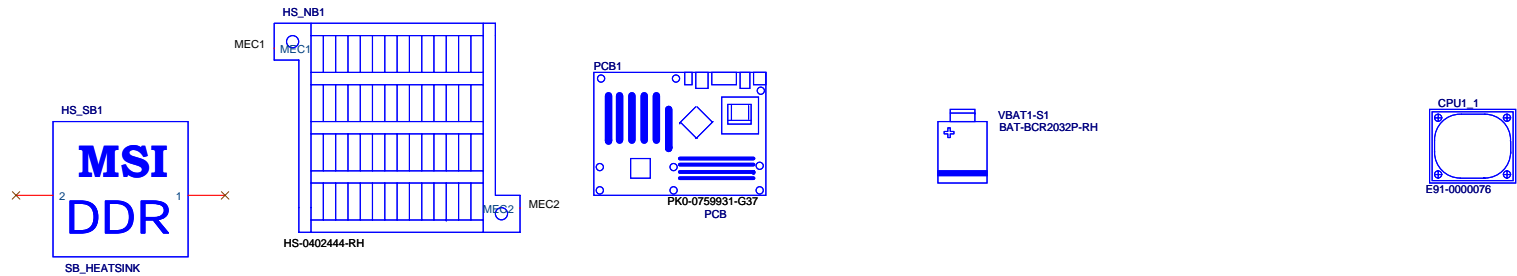


Figure 1 shows three LED driver circuit diagrams. (a) LED1 and LED2 driver: A MOSFET (78V2N7000ZDF-F, SOT363-6-RH) is used. The gate is driven by OC_LED1# and OC2BTL_LED1#. The drain is connected to LED1 and LED2. (b) LED3 and LED4 driver: A MOSFET (47K9R0402) is used. The gate is driven by OC1_SMB# and OC1_GEAR1#. The drain is connected to LED3 and LED4. (c) LED5 and LED6 driver: A MOSFET (330R0402) is used. The gate is driven by OC1_SMB# and OC1_GEAR1#. The drain is connected to LED5 and LED6.

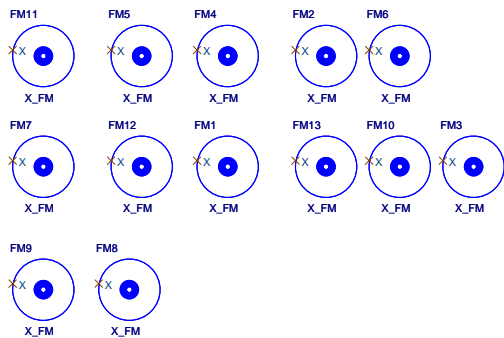


Intel Front Panel

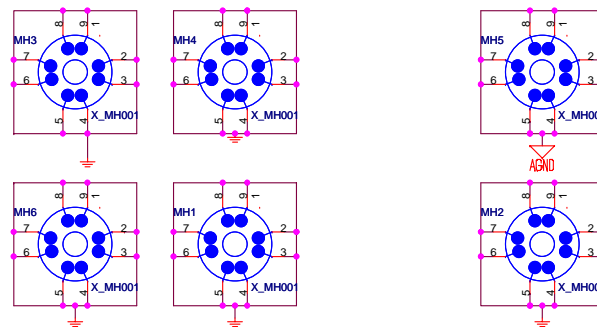




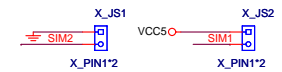
Optics Orientation Holes



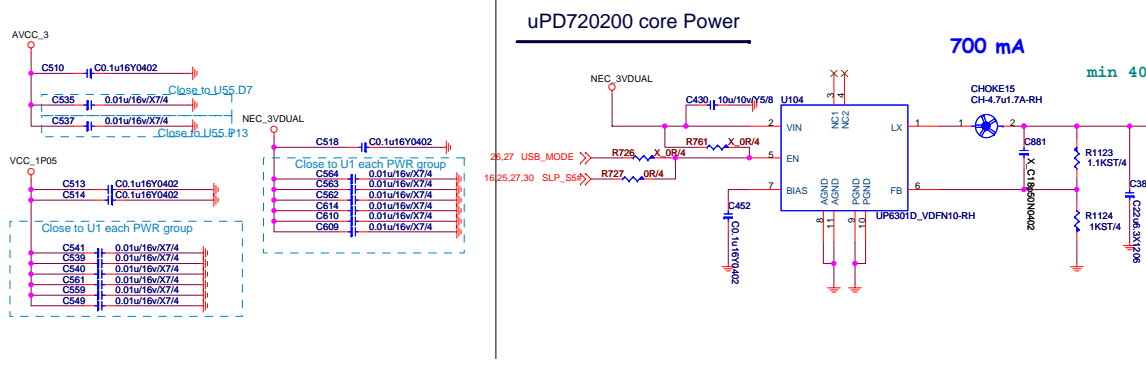
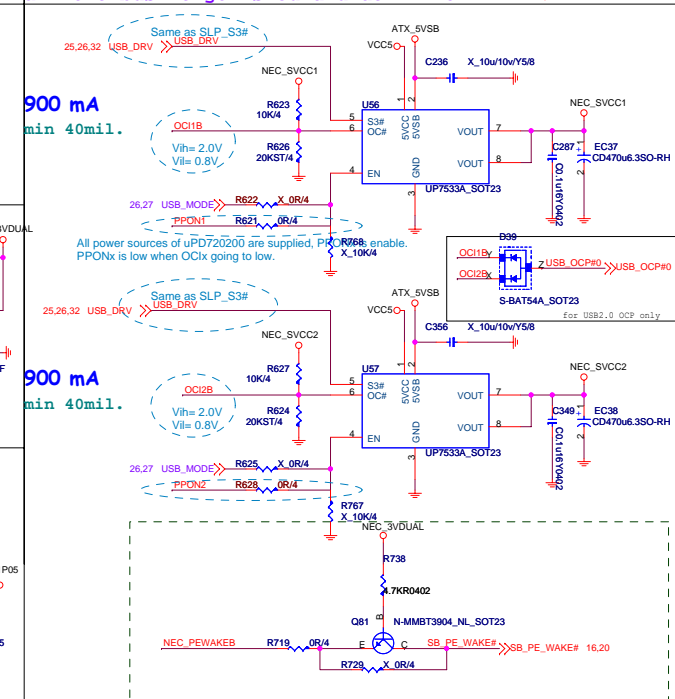
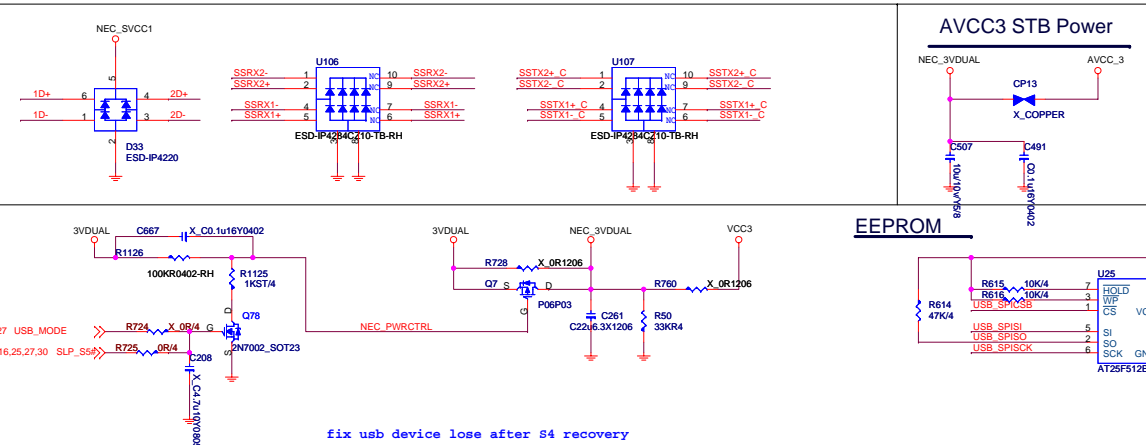
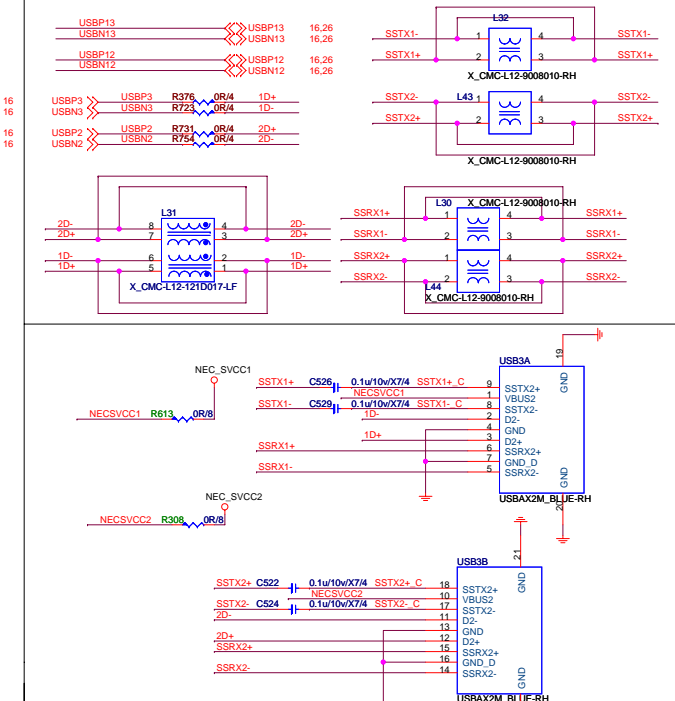
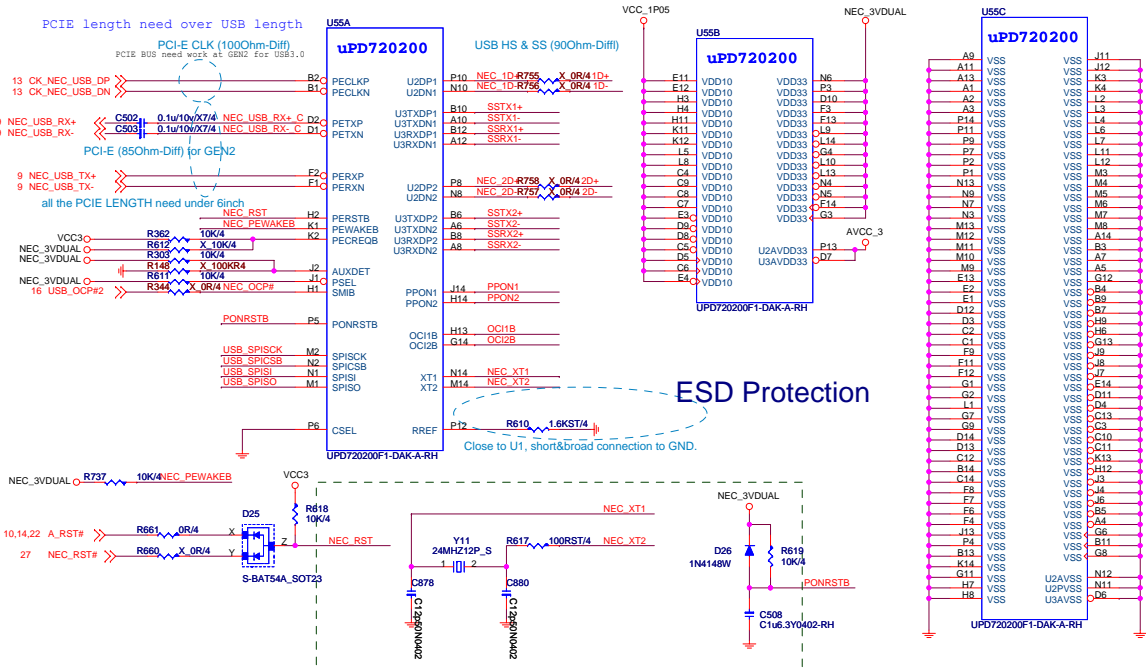
Mounting Holes



Simulation



Micro Star Restricted Secret		
Title	MANUAL PARTS	Rev 10
Document Number	MS-7599	
MICRO-STAR INT'L CO., LTD. No. 69, Li-De St, Jung-He City, Taipei Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, March 02, 2010 Sheet 31 of 38



Micro Star Restricted Secret		
Title	NEC720200 USB3.0	Rev 10
Document Number	MS-7599	
MICRO-STAR INT'L CO. LTD. No. 69, Li-De St, Jung-Hsue City, Taipex Hsien, Taiwan http://www.msi.com.tw		Last Revision Date: Tuesday, March 02, 2010 Sheet 33 of 38